CLAIMS:

What is claimed is:

1. An interposer comprising:

a substrate having first and second opposed sides with a first set of terminals on the first side, a second set of terminals on the second side, and a means of electrically interconnecting the terminals of the first and second sides;

a first set of resilient contact structures, each having a portion connected to a respective one of the terminals of the first set of terminals, a first contact region distant from the substrate, and an elongate section extending from the portion to the first contact region, the elongate section resiliently bending upon depression of the first contact region towards the substrate; and

a second set of resilient contact structures, each having a portion attached to a respective one of the terminals of the second set of terminals, a contact region distant from the substrate, and an elongate section extending from the portion to the contact region, the elongate section resiliently bending upon depression of the contact region towards the substrate,

wherein upon depression of the first and second contact regions, the interposer causes electrical coupling of two devices.

2. An interposer as recited in claim 1 wherein said first set of resilient contact structures are offset in position from said second set of resilient contact structures

3. An interposer as recited in claim 1 further including components disposed on said substrate.

4. An interposer as recited in claim 3 wherein said components are passive components.

5. An interposer as recited in claim 4 wherein said passive components are capacitors.

6. An interposer as recited in claim 4 wherein said components are active components.

7. An interposer as recited in claim 1 wherein said substrate is formed of silicon.

8. An interposer as recited in claim 1 wherein said substrate is formed of metallic material.

9. An interposer as recited in claim 1 wherein said substrate is formed of organic material.

10. An interposer as recited in claim 1 wherein said substrate is formed of ceramic material.

11. An interposer as recited in claim 1 wherein said substrate includes power and ground planes.

12. An interposer as recited in claim 1 wherein said substrate includes multiple wiring layers.

13. An interposer as recited in claim 1 wherein said first set of resilient contact structures are formed lithographically.

14. An interposer as recited in claim 1 wherein said second set of resilient contact structures are formed lithographically.

15. An interposer as recited in claim 1 wherein said first set of resilient contact structures are formed by bonding and plating.

16. An interposer as recited in claim 1 wherein said second set of resilient contact structures are formed by bonding and plating.

17. An interposer as recited in claim 1 wherein an overtravel stop is disposed on said first side of said substrate for controlling compression of said first set of resilient contact structures upon depression of the first contact region.

18. An interposer as recited in claim 1 wherein a first overtravel stop is disposed on said first side of said substrate for controlling compression of said first set of resilient contact structures upon depression of the first contact region and further wherein a second overtravel stop is disposed on said second side of said substrate for controlling compression of said second set of resilient contact structures upon depression of the second contact region.

19. An interposer as recited in claim 1 wherein said first and second set of resilient contact structures comprise resilient spring structures.

20. An interposer as recited in claim 1 wherein said first set of contact structures comprise solder balls.

21. An interposer as recited in claim 20 wherein said second plurality of contact structures comprise resilient spring structures.

22. An interposer as recited in claim 1 wherein said interposer is part of a wafer-level test assembly.

23. An interposer as recited in claim 1 wherein contact elements of said interposer are formed lithographically.

24. An interposer as recited in claim 1 wherein through-holes are formed on said substrate.

25. An interposer as recited in claim 1 wherein said substrate is substantially rigid.

26. An interposer as recited in claim 1 wherein said substrate is substantially flexible.

27. A method for testing a wafer comprising:

connecting a first side of an interposer having a first plurality of resilient contact elements disposed thereon to the wafer;

connecting a second side of an interposer having a second plurality of resilient contact elements disposed thereon to a wiring substrate ; and

providing signals to the wiring substrate thereby causing testing of the wafer.

28. A method for forming an interposer comprising:

providing a substrate having a first surface and a second surface, said second surface being opposite of said first surface;

forming a first plurality of contact elements on said first surface of said substrate; and

forming a second plurality of contact elements on said second surface of said substrate.

29. A method as recited in claim 28 further including the step of forming through-hole terminals in said substrate.

30. A method for performing wafer-level burn-in and test of a plurality of semiconductor devices (DUTs) resident on a semiconductor wafer, comprising:

providing a plurality of active electronic components having terminals on a surface thereof; and

providing an interposer for effecting direct electrical connections between terminals of the plurality of DUTs and the terminals of the active electronic components.

31. An assembly for electrically connecting a first electronic component to a second electronic component comprising:

an interposer having a substrate having a first surface and a second surface, said first surface having a first set of resilient contact structures and said second surface having a second set of resilient contact structures, the first and second electronic components having capture pads on their respective surfaces, configured to mate with corresponding first and second sets of resilient contact structures; and a housing connected to secure the first and second electronic components to the interposer.

32. A system for testing a wafer comprising:

an interposer;

a wiring layer; and

means for connecting the wafer to the wiring layer using the interposer thereby causing testing of the wafer.

33. A system as recited in claim 32 further including active components mounted to the wiring layer.

34. A method for testing a semiconductor wafer comprising:

providing a wafer-under-test;

providing a wiring layer being part of a wafer test system; and

connecting an interposer having an upper surface and a lower surface and having a plurality of resilient contact elements mounted on each of said upper and lower surfaces, between the wafer-under-test and the wiring layer, such connection being provided by the plurality of resilient contact elements.

35. A method for testing as recited in claim 34 wherein providing a plurality of devices on the wafer-under-test and exercising the devices at elevated temperatures.